

TVS Diode

Transient Voltage Suppressor Diodes

ESD208-B1-02 Series

Ultra Low Clamping ESD / Transient Protection Diode

ESD208-B1-02EL
ESD208-B1-02ELS

Data Sheet

Revision 1.2, 2013-11-29
Final

Power Management & Multimarket

Revision History Revision 1.1, 2013-11-26

| Page or Item | Subjects (major changes since previous revision) |
|---------------------------------|--|
| Revision 1.2, 2013-11-29 | |
| 5 | Update of Table 2-2) |
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Last Trademarks Update 2010-10-26

1 Ultra Low Clamping ESD / Transient Protection Diode

1.1 Features

- ESD / transient protection of signal lines in low voltage applications according to:
 - IEC61000-4-2 (ESD): **±30 kV air discharge, ±25 kV contact discharge**
 - IEC61000-4-4 (EFT): **±80 A / ±4 kV (5/50 ns)**
 - IEC61000-4-5 (Surge): **±4 A (8/20 μs)**
- Bi-directional, symmetrical working voltage up to $V_{RWM} = \pm 3.3\text{ V}$
- Low capacitance: $C_L = 6\text{ pF}$ (typical)
- Very low clamping voltage due to extremely low dynamic resistance down to: $R_{DYN} = 0.2\ \Omega$ (typical)
- Pb-free (RoHS compliant) and halogen free package, very small form factor down to: 0.62 x 0.32 x 0.31 mm³



1.2 Application Examples

- Keypad, touchpad, buttons, convenience keys
- LCD displays, Camera, audio lines, mobile communication, Consumer products (E-Book, MP3, DVD, DSC...)
- Notebooks tablets and desktop computers and their peripherals

1.3 Product Description

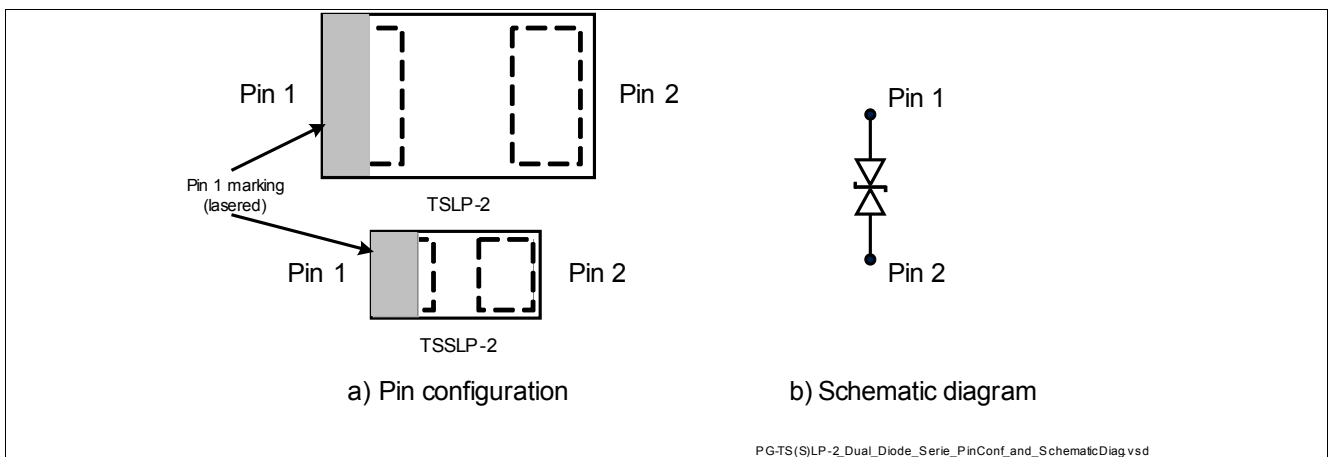


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Ordering Information

| Type | Package | Configuration | Marking code |
|-----------------|-----------|------------------------|--------------|
| ESD208-B1-02EL | TSLP-2-19 | 1 line, bi-directional | C |
| ESD208-B1-02ELS | TSSLP-2-3 | 1 line, bi-directional | <u>C</u> |

2 Characteristics

Table 2-1 Maximum Ratings at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified ¹⁾

| Parameter | Symbol | Values | | | Unit |
|--|-----------|--------|------|----------|------------------|
| | | Min. | Typ. | Max. | |
| ESD discharge ²⁾ air contact | V_{ESD} | – | – | 30 25 | kV |
| Peak pulse current ($t_p = 8/20\text{ }\mu\text{s}$) ³⁾ | I_{PP} | – | – | 4 | A |
| Peak pulse power ($t_p = 8/20\text{ }\mu\text{s}$) ³⁾ | P_{PK} | – | – | 30 | W |
| Operating temperature range | T_{OP} | -55 | – | 125 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -65 | – | 150 | $^\circ\text{C}$ |

- 1) Device is electrically symmetrical
- 2) V_{ESD} according to IEC61000-4-2 ($R = 330\text{ }\Omega$, $C = 150\text{ pF}$)
- 3) I_{PP} according to IEC61000-4-5 ($t_p = 8/20\text{ }\mu\text{s}$)

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

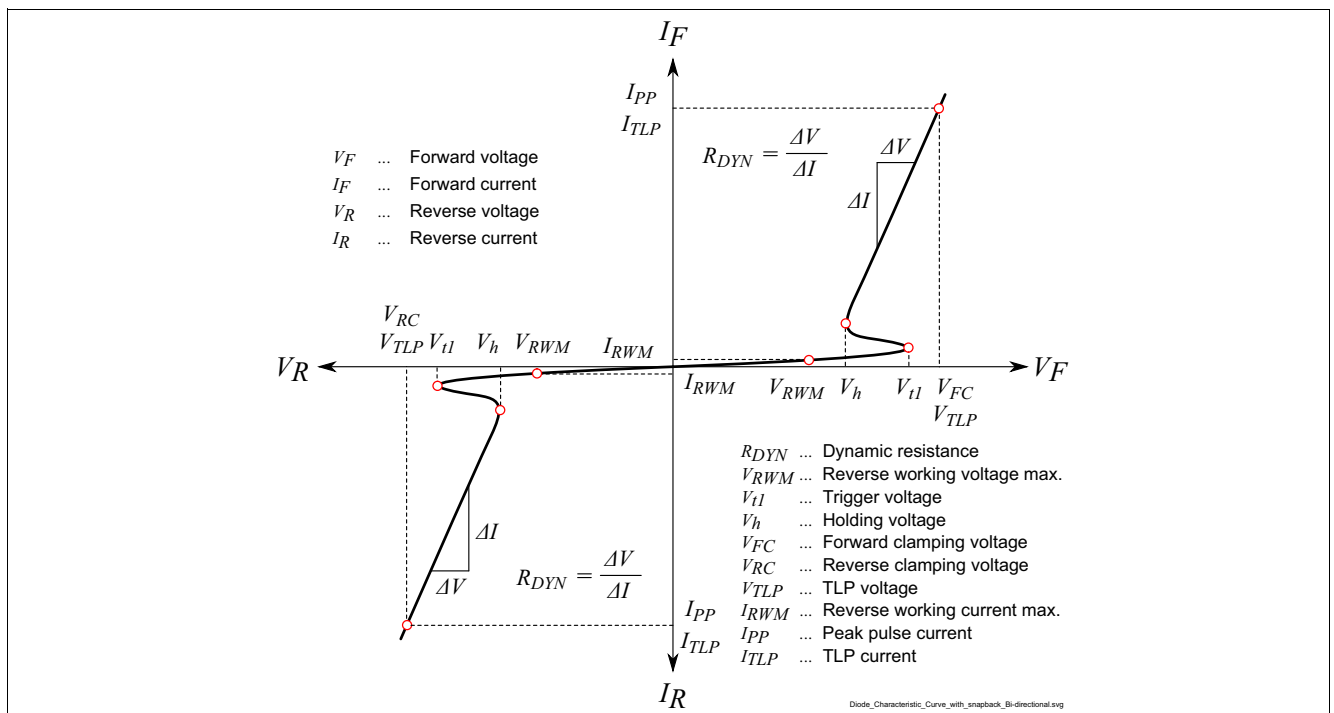


Figure 2-1 Definitions of electrical characteristics

Table 2-2 DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified ¹⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Reverse working voltage | V_{RWM} | – | – | 3.3 | V | |
| Reverse current | I_R | – | <10 | 50 | nA | $V_R = 3.3\text{ V}$ |
| Trigger voltage | V_{t1} | 3.65 | – | – | V | |
| Holding voltage | V_h | 3.65 | 4 | – | V | $I_R = 10\text{ mA}$ |

1) Device is electrically symmetrical

Table 2-3 AC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|------------------|--------|--------|------|------|------|--------------------------------------|
| | | Min. | Typ. | Max. | | |
| Line capacitance | C_L | – | 6 | 9 | pF | $V_R = 0\text{ V}, f = 1\text{ MHz}$ |
| | | | 6 | 9 | | $V_R = 0\text{ V}, f = 1\text{ GHz}$ |

Table 2-4 ESD and Surge Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified ¹⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|-----------|--------|------|------|----------|--|
| | | Min. | Typ. | Max. | | |
| Clamping voltage ²⁾ | V_{CL} | – | 8 | 9.5 | V | $I_{TLP} = 16\text{ A}, t_p = 100\text{ ns}$ |
| | | – | 11 | 12.5 | | $I_{TLP} = 30\text{ A}, t_p = 100\text{ ns}$ |
| Clamping voltage ³⁾ | | – | 4.8 | 6.3 | | $I_{PP} = 1\text{ A}, t_p = 8/20\text{ }\mu\text{s}$ |
| | | – | 5.8 | 7.3 | | $I_{PP} = 3\text{ A}, t_p = 8/20\text{ }\mu\text{s}$ |
| | | – | 6.6 | 8.1 | | $I_{PP} = 4\text{ A}, t_p = 8/20\text{ }\mu\text{s}$ |
| Dynamic resistance ²⁾ | R_{DYN} | – | 0.20 | 0.25 | Ω | $t_p = 100\text{ ns}$ |

1) Device is electrically symmetrical

2) Please refer to Application Note AN210 [1] TLP parameters: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$, averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{TLP1} = 10\text{ A}$ and $I_{TLP2} = 40\text{ A}$.

3) I_{PP} according to IEC61000-4-5 ($t_p = 8/20\text{ }\mu\text{s}$)

Typical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

3 Typical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

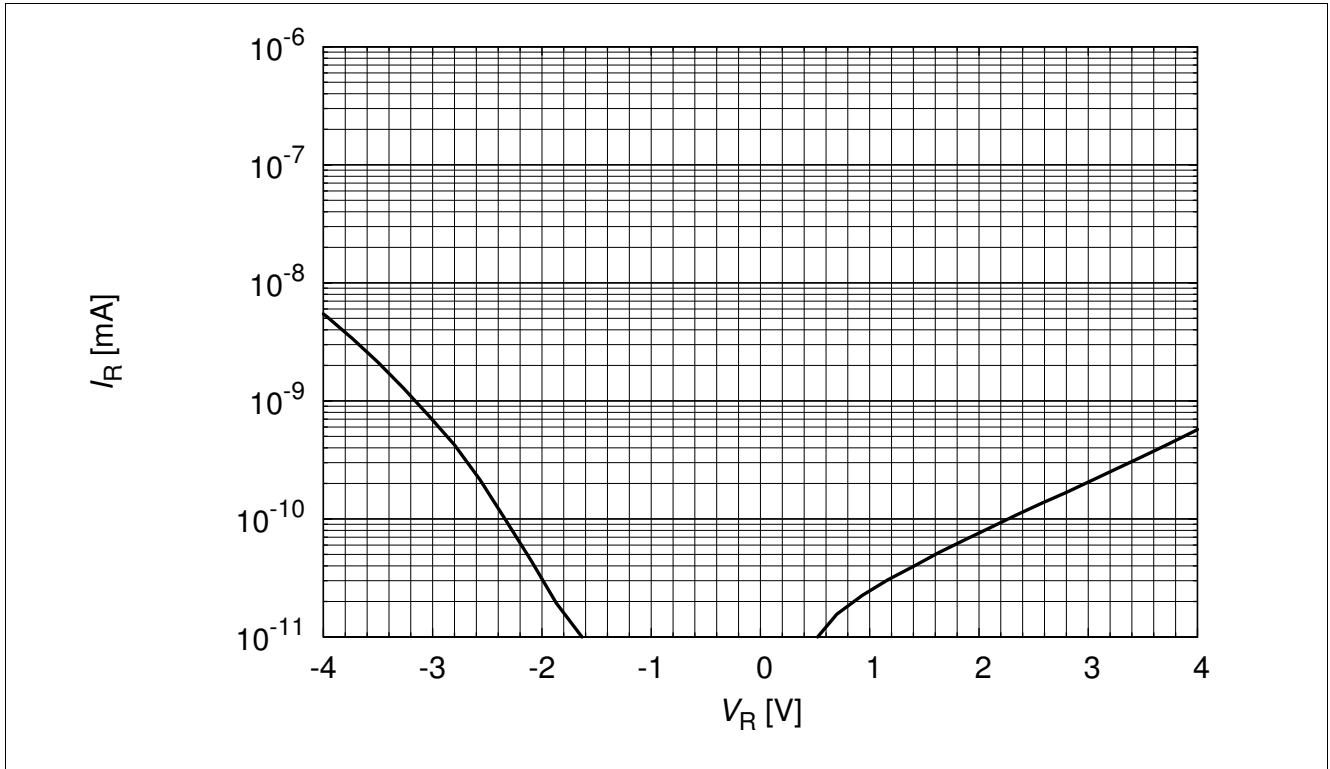


Figure 3-1 Reverse current: $I_R = f(V_R)$

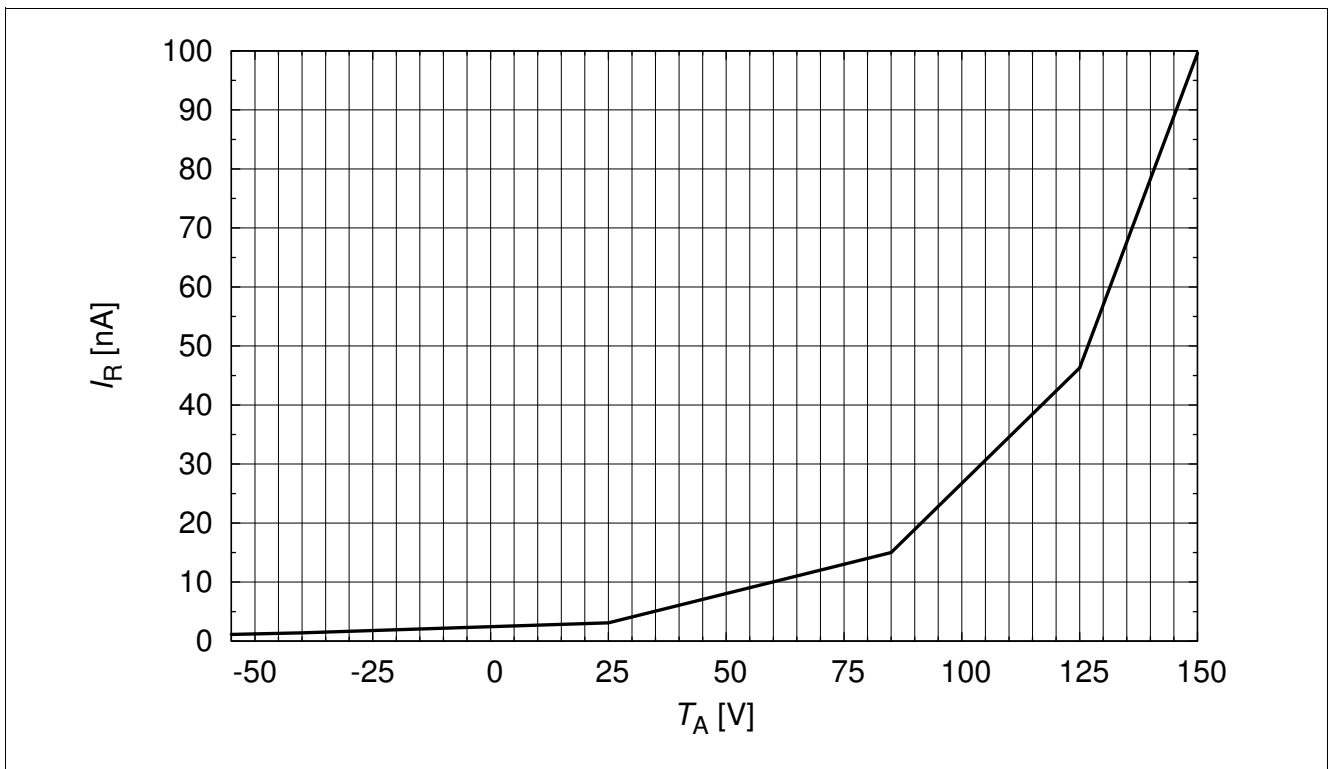


Figure 3-2 Reverse current: $I_R = f(T_A)$, $V_R = 3.3\text{ V}$

Typical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

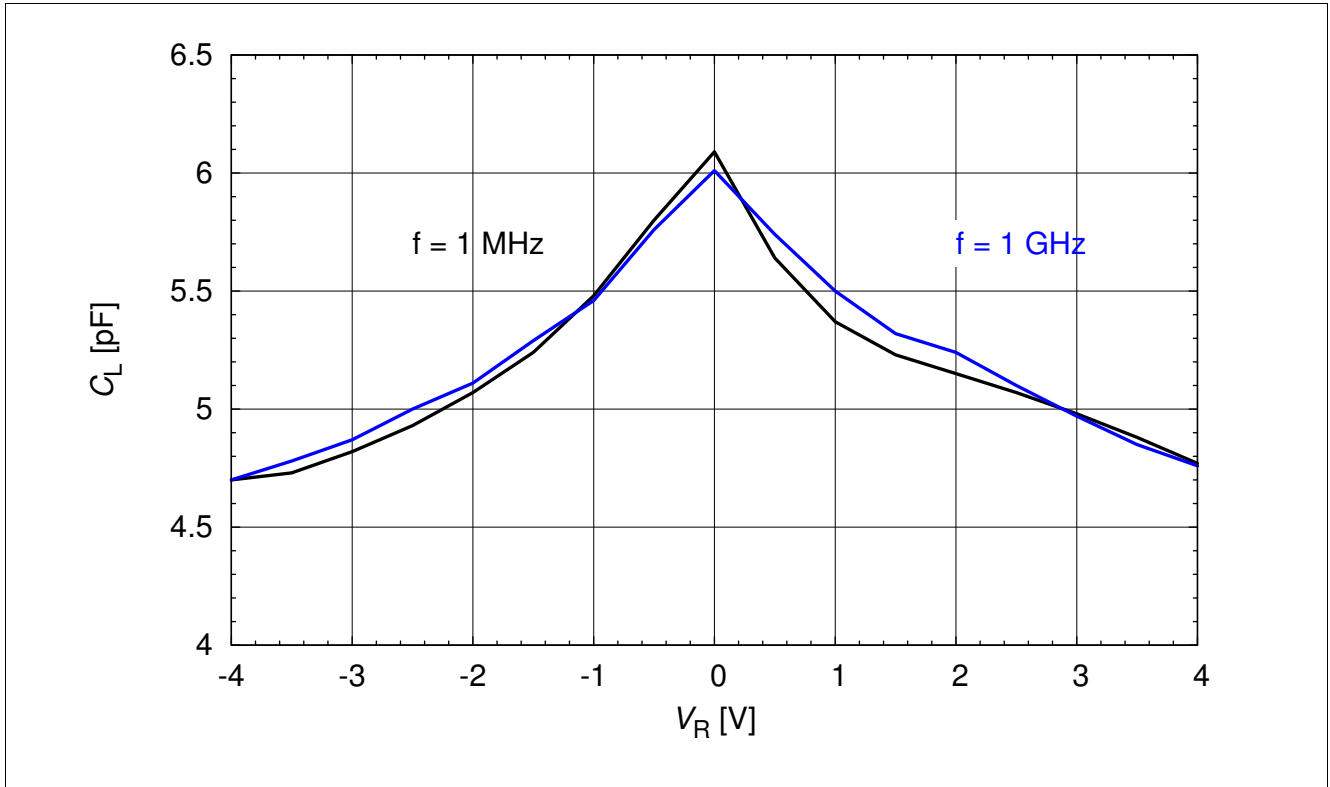


Figure 3-3 Line capacitance: $C_L = f(V_R)$

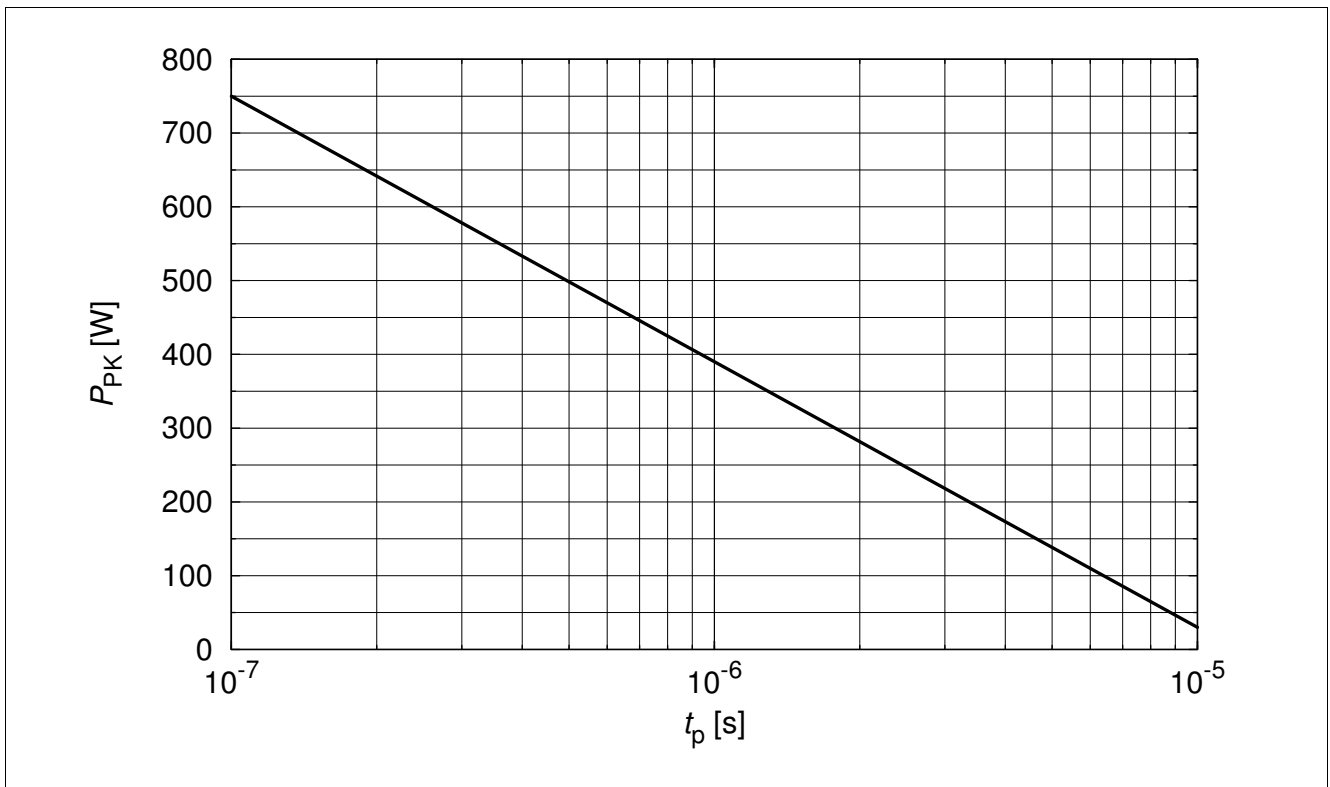


Figure 3-4 Peak pulse power: $P_{PK} = f(t_p)$

Typical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

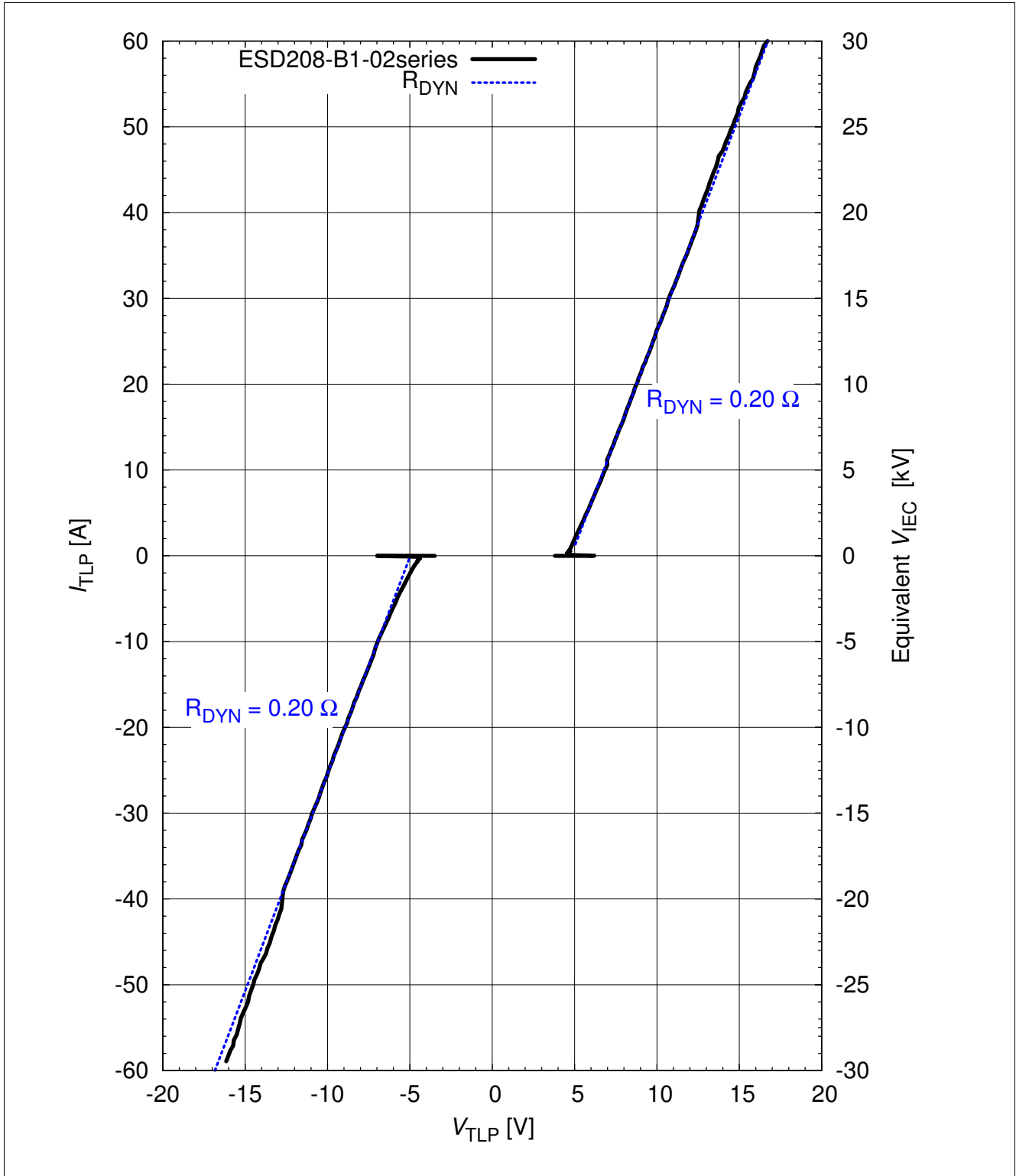


Figure 3-5 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$, I_{TLP} and V_{TLP} averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using squares fit to TLP characteristics between $I_{TLP1} = 10\text{ A}$ and $I_{TLP2} = 40\text{ A}$. Please refer to Application Note AN210 [1]

Typical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

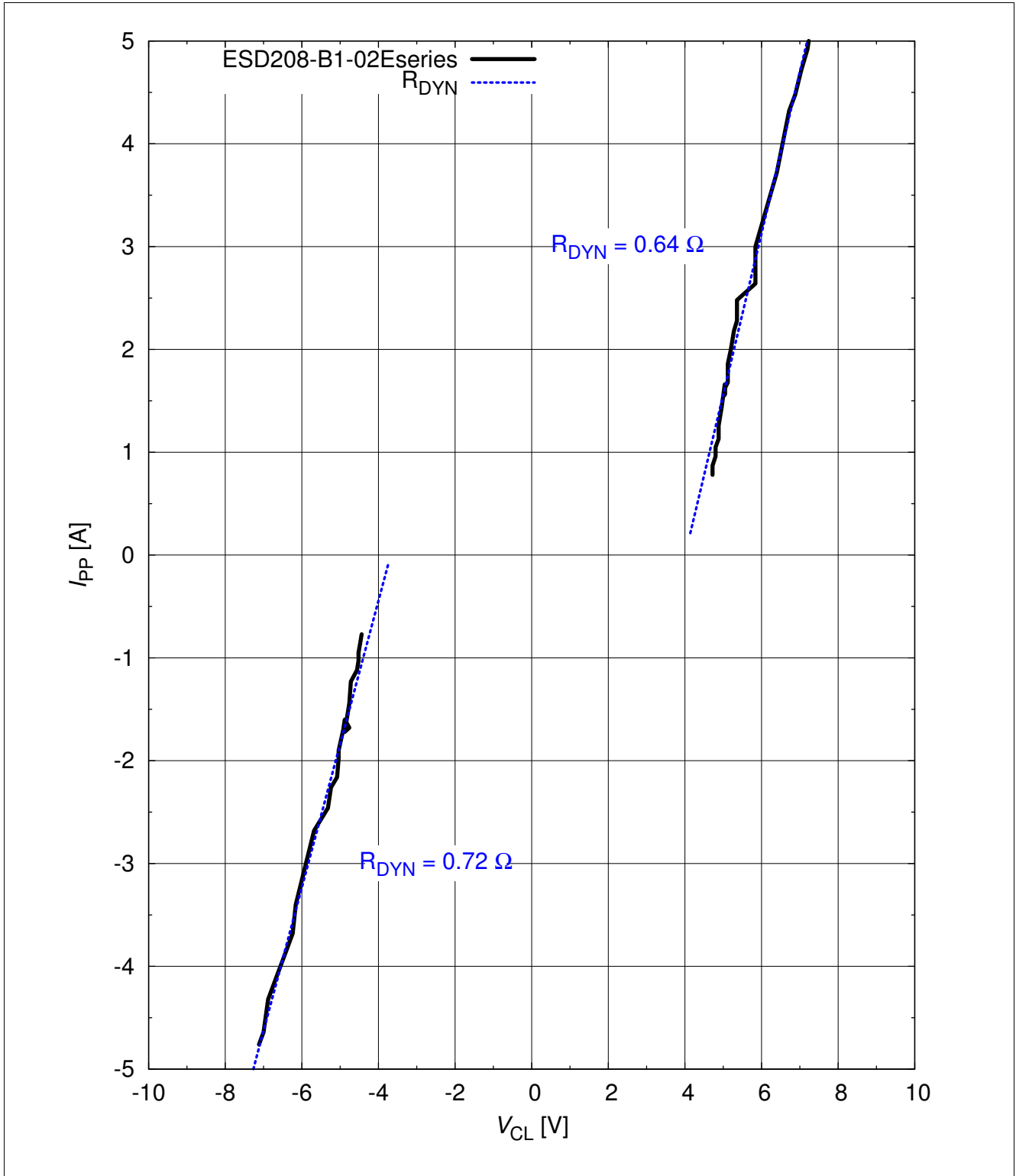


Figure 3-6 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$

Typical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

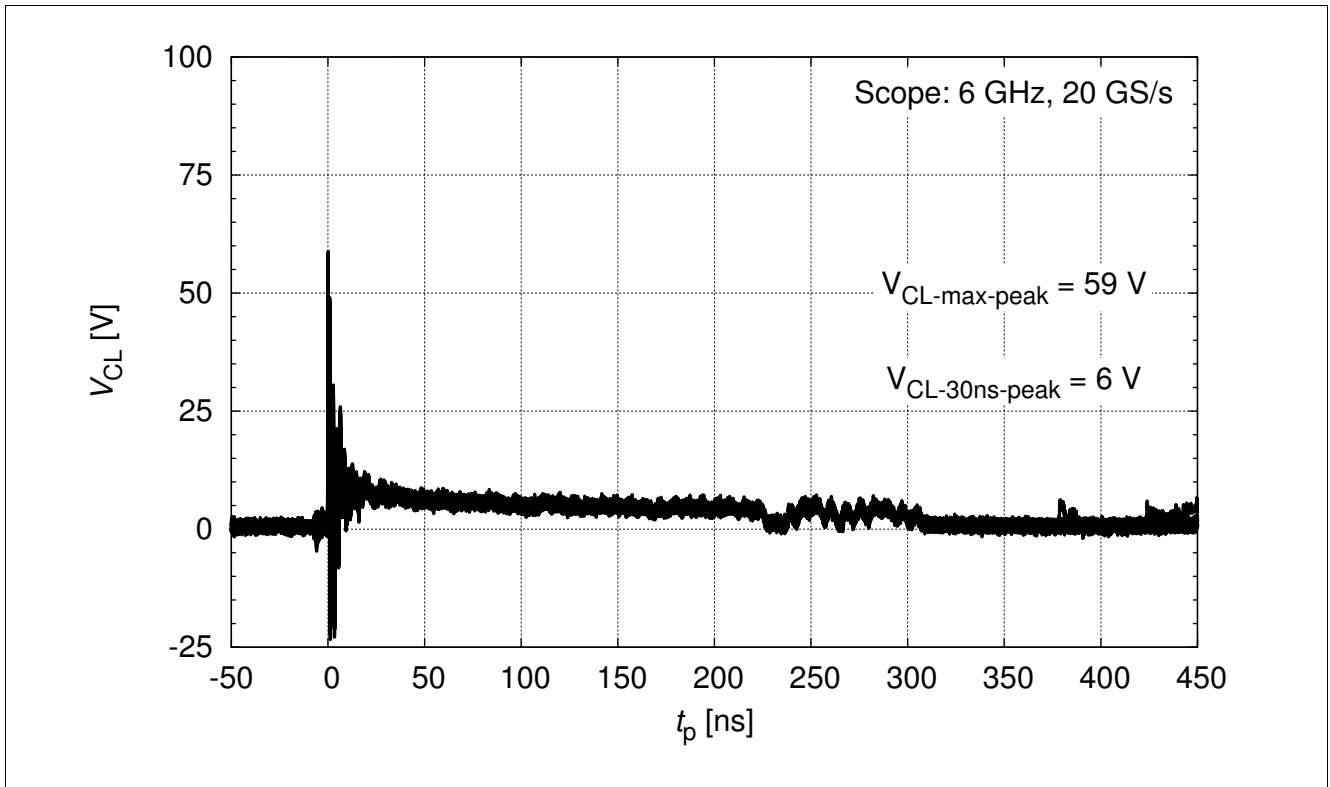


Figure 3-7 IEC61000-4-2 : $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

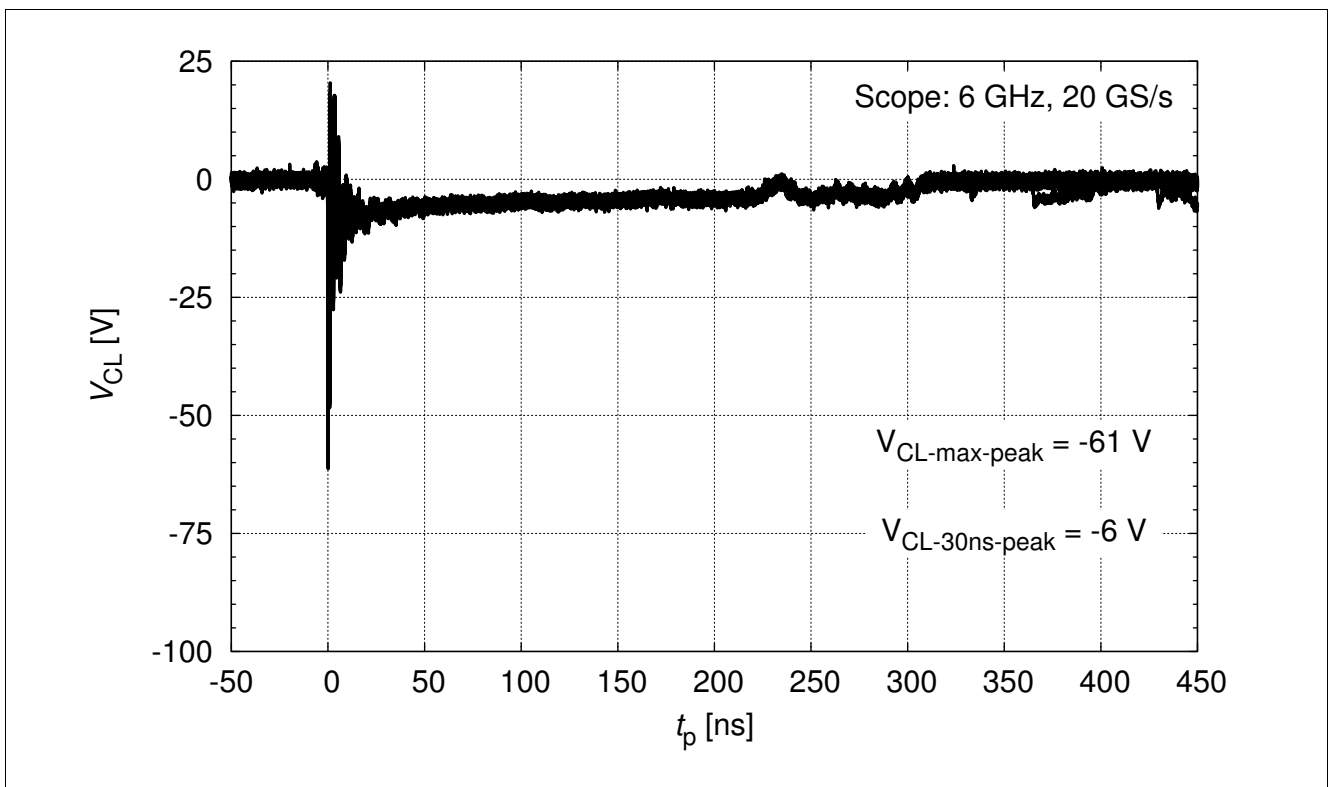


Figure 3-8 IEC61000-4-2 : $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

Typical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

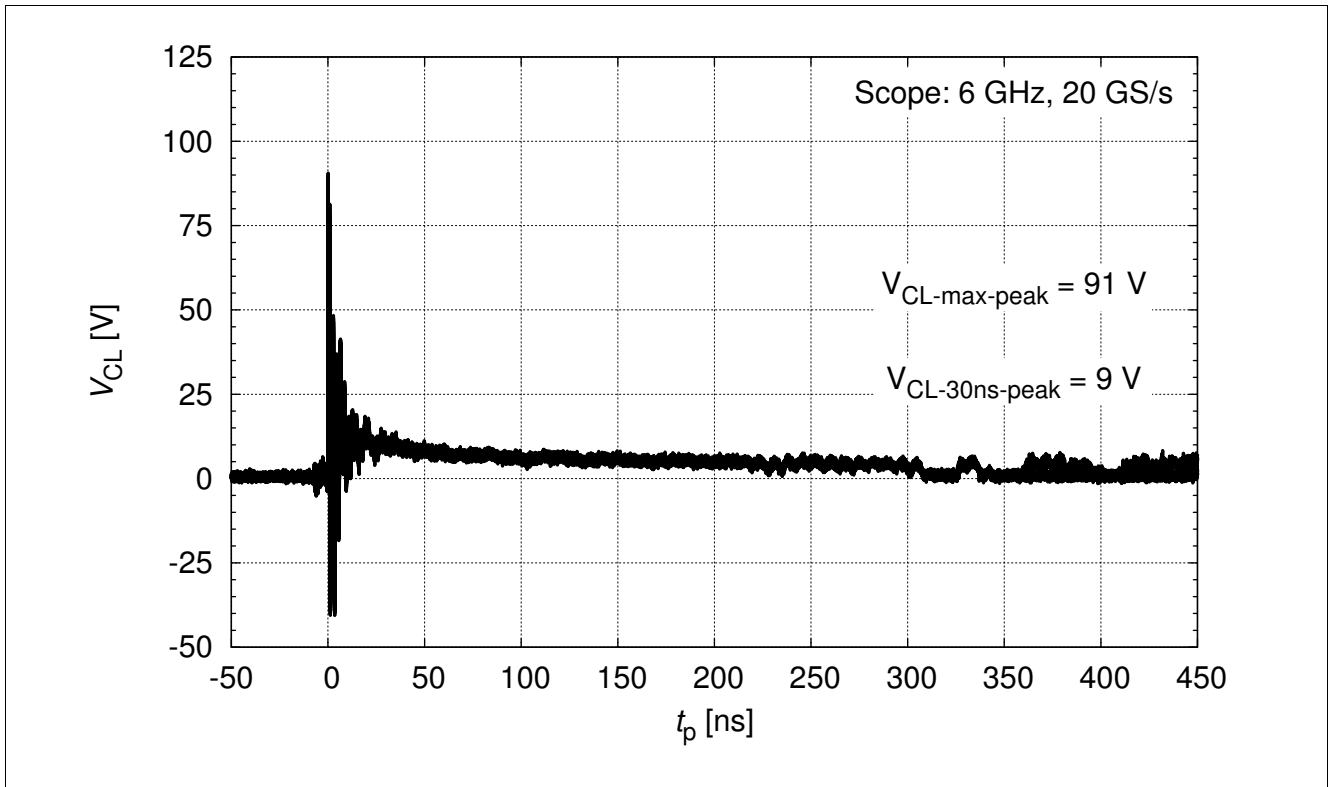


Figure 3-9 IEC61000-4-2 : $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

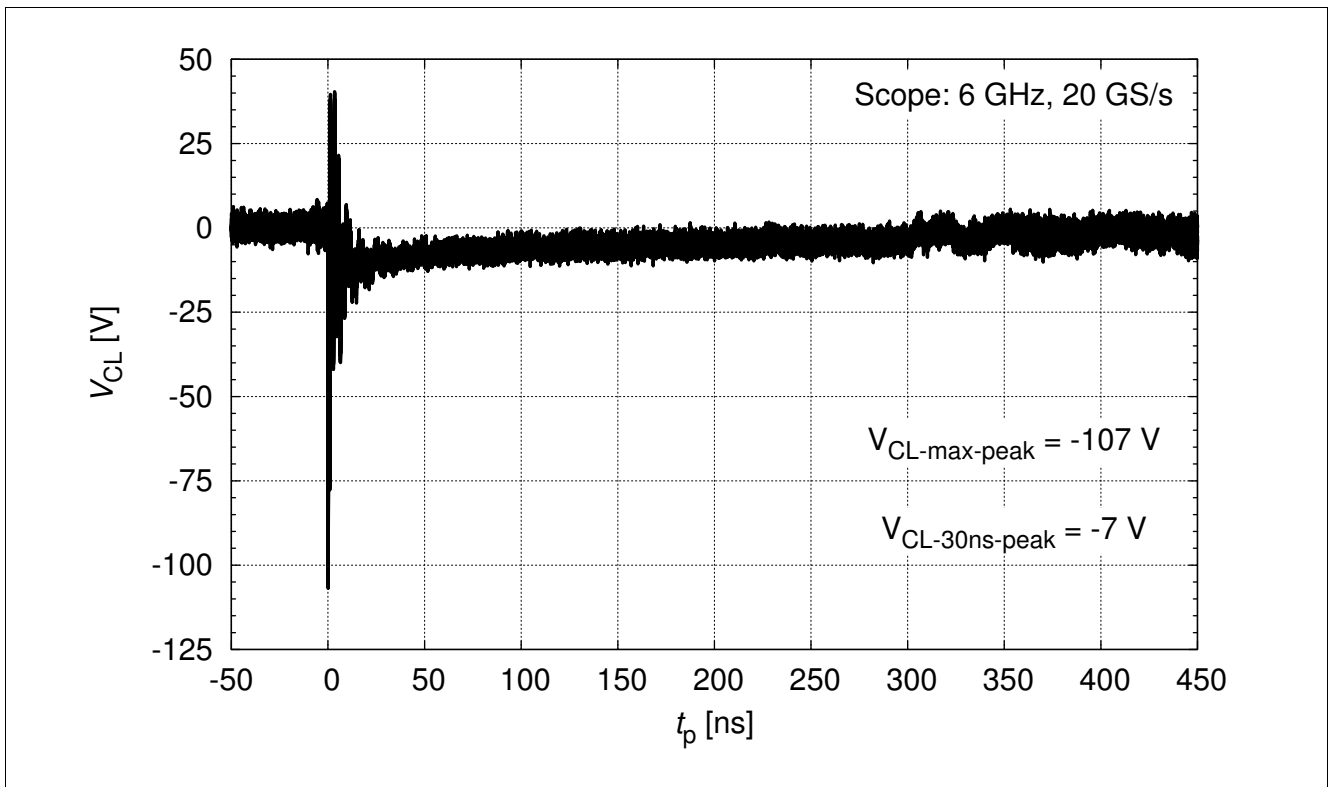


Figure 3-10 IEC61000-4-2 : $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

4 Application Information

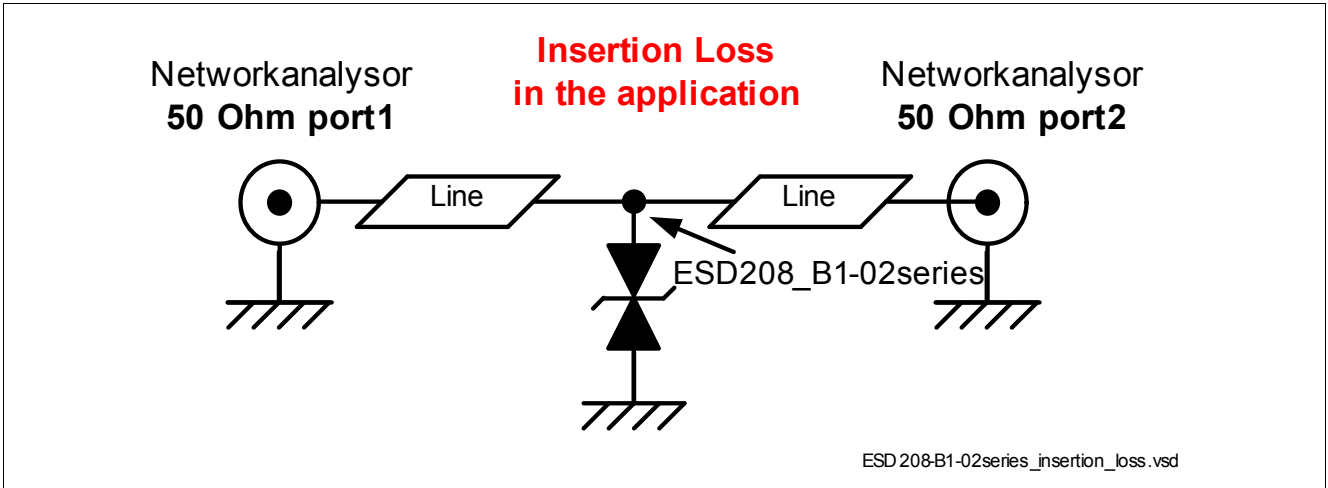


Figure 4-1 Insertion loss measured in 50 Ω environment

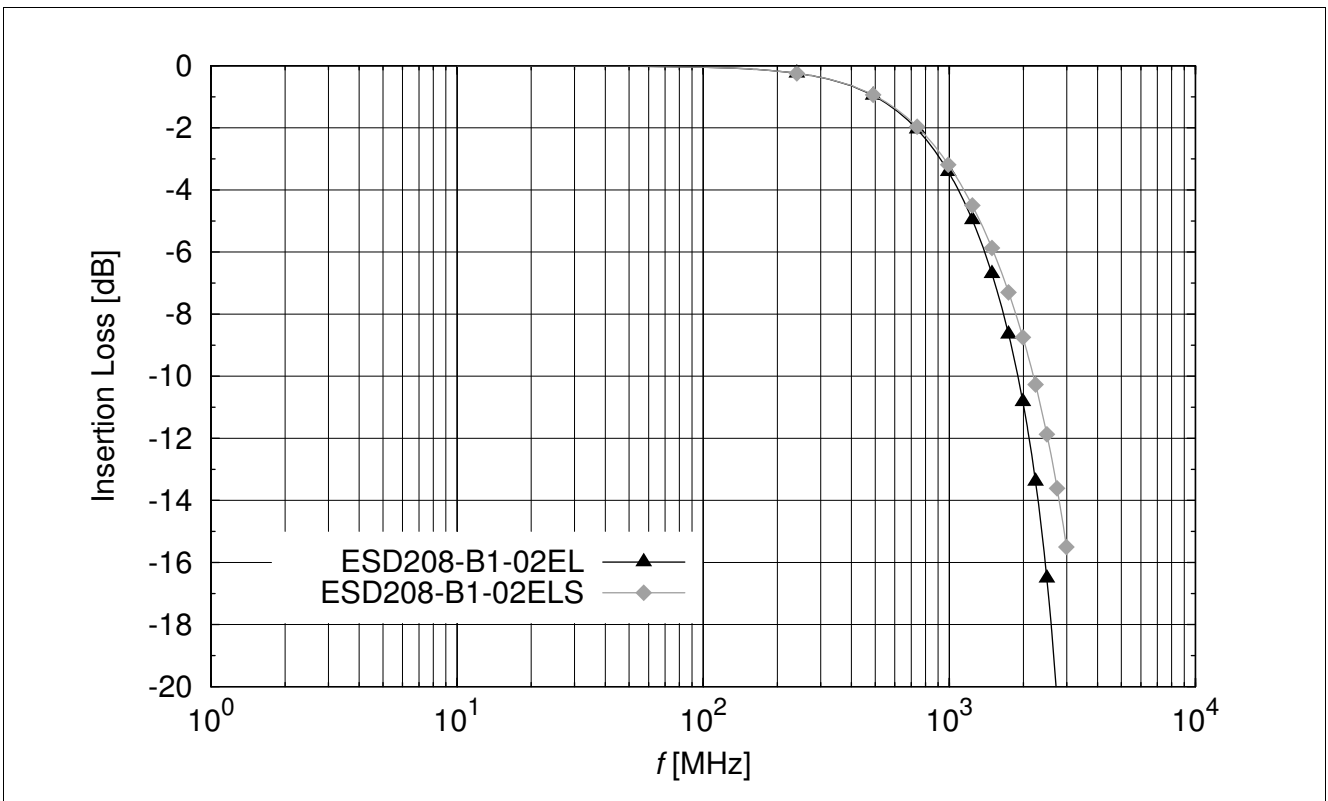


Figure 4-2 Insertion loss vs. frequency of ESD208-B1-02xx in a 50 Ω system

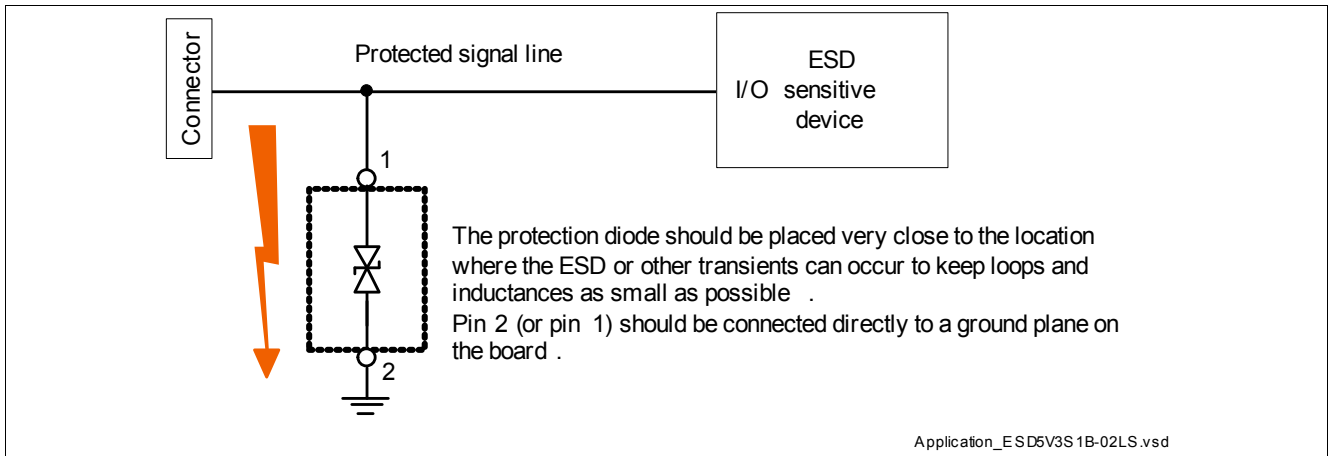


Figure 4-3 Single line, bi-directional ESD / Transient protection

5 Package Information

5.1 TSLP-2-19

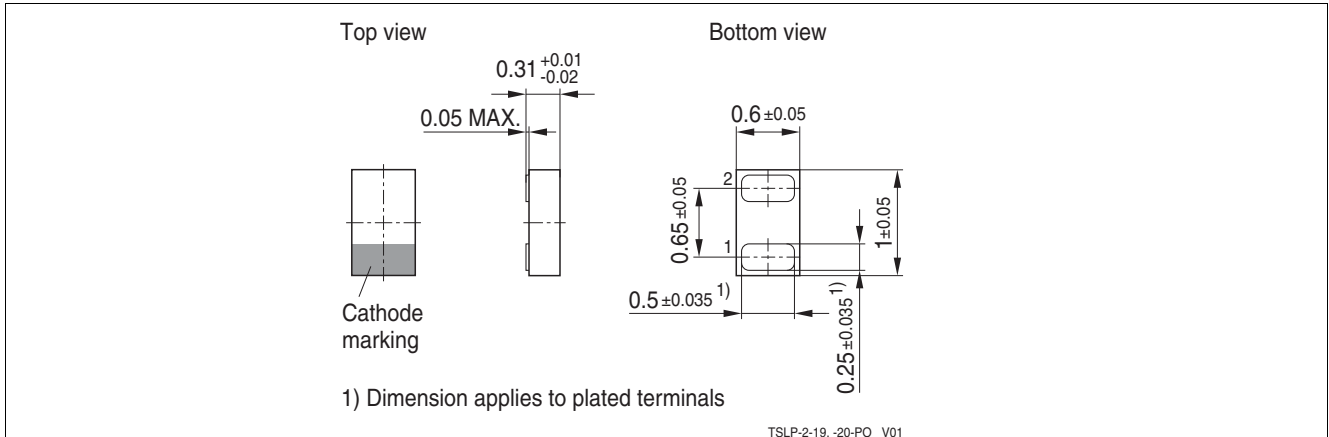


Figure 5-1 TSLP-2-19: Package overview (dimension in mm)

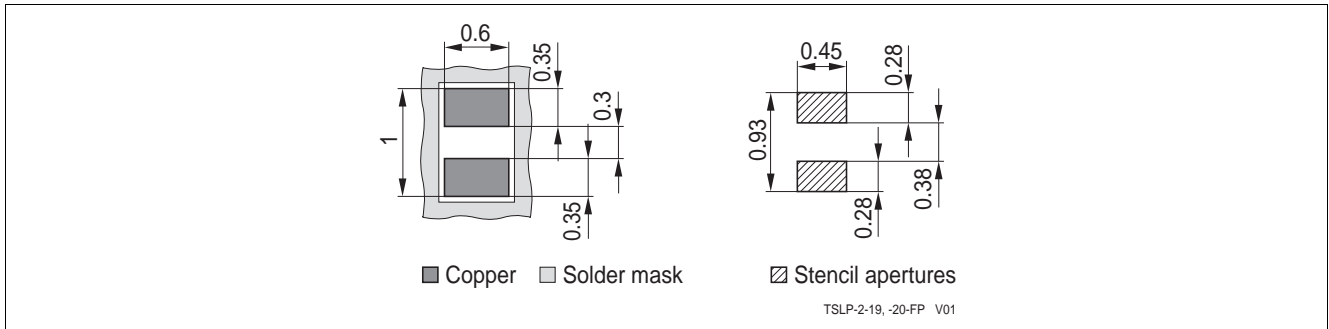


Figure 5-2 TSLP-2-19: Footprint (dimension in mm)

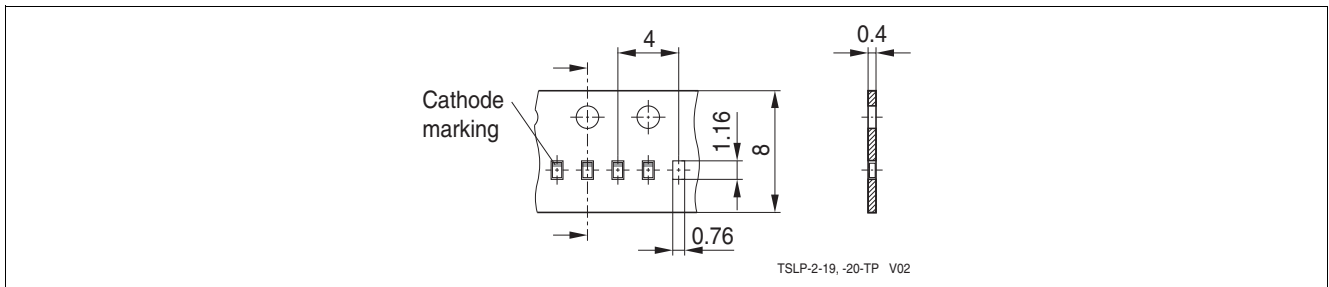


Figure 5-3 TSLP-2-19: Tape information (dimension in mm)

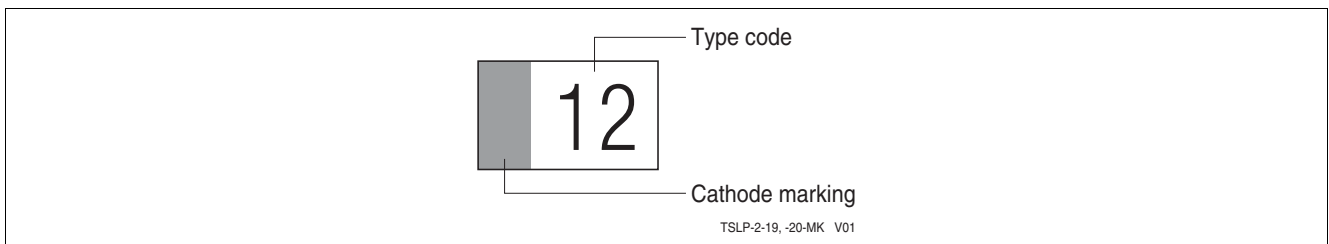


Figure 5-4 TSLP-2-19: Marking (example)

5.2 TSSLP-2-3

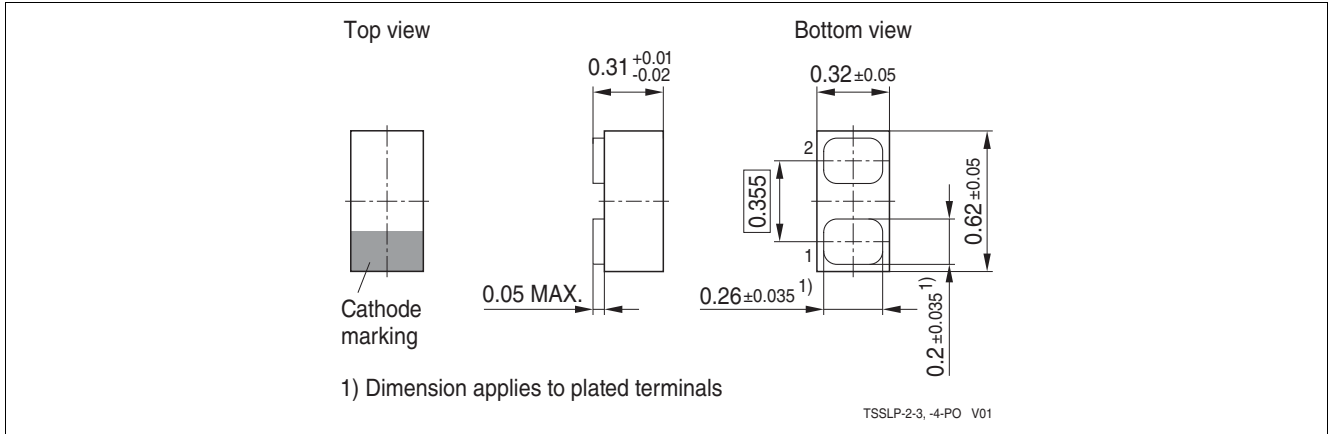


Figure 5-5 TSSLP-2-3: Package outline(dimension in mm)

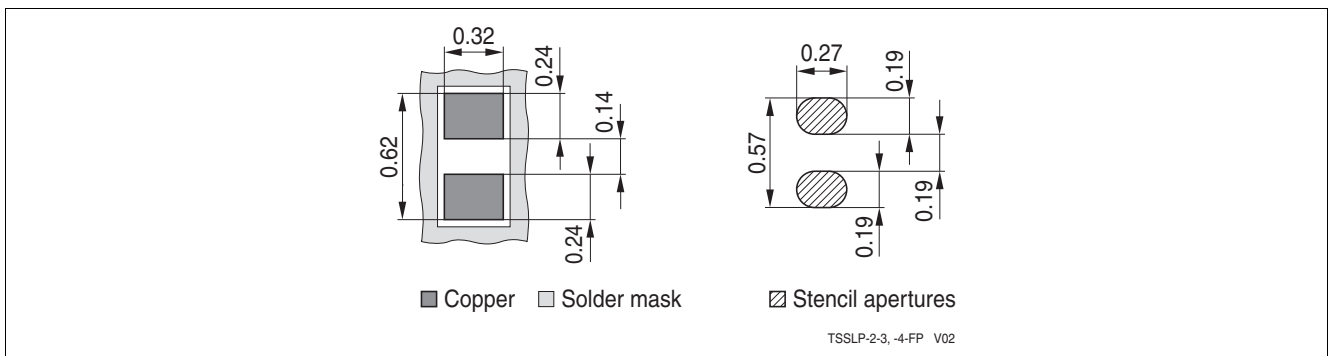


Figure 5-6 TSSLP-2-3: Footprint (dimension in mm)

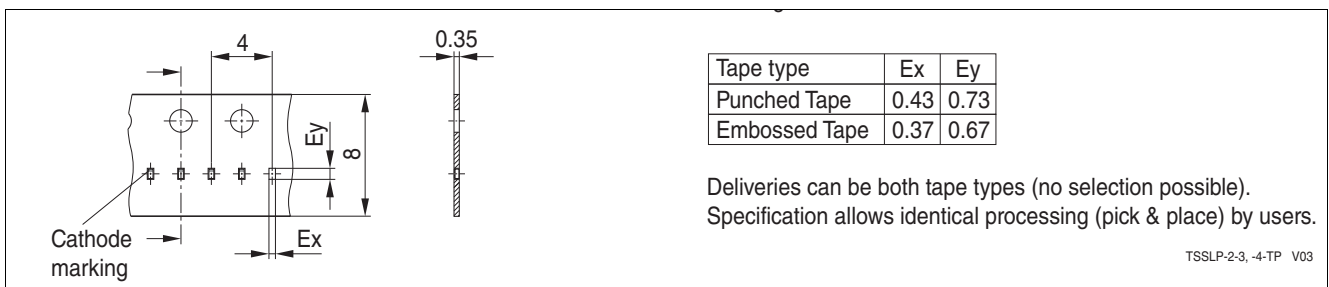


Figure 5-7 TSSLP-2-3: Tape information (dimension in mm)

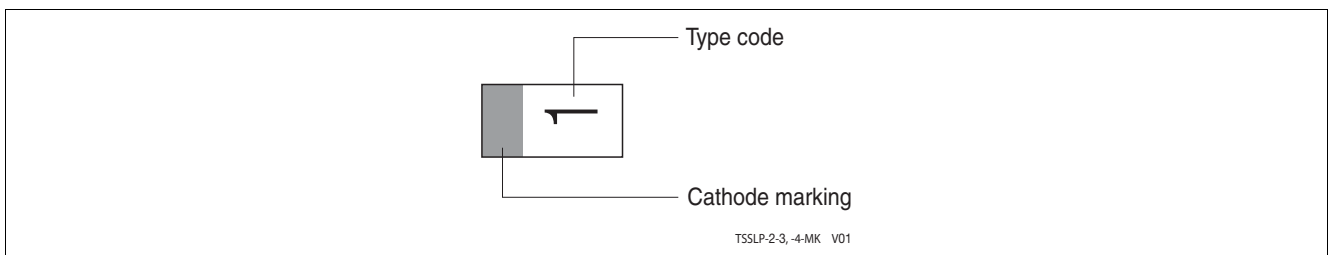


Figure 5-8 TSSLP-2-3: Marking (example)

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

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